Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A non-volatile memory device comprising:

an organic ambipolar semiconductor layer in contact with at least two sides of a first electrode and a second electrode; and

an organic ferroelectric layer in contact with one side of each of the first electrode and the second electrode and at least two sides of a control electrode, said organic ambipolar semiconductor layer and said organic ferroelectric layer being at least partially in contact with each other.

2. (Currently amended) The non-volatile memory device according to claim 1, ~~furthermore comprising a~~wherein the control electrode ~~being~~ is formed in a first conductive layer.

3. (Previously presented) The non-volatile memory device according to claim 2, the control electrode being separated from

said organic ambipolar semiconductor layer by said organic ferroelectric layer.

4. (Currently amended) The non-volatile memory device according to claim 2, ~~furthermore comprising a~~wherein the first ~~main~~ electrode and ~~a~~ the second ~~main~~ electrode ~~being~~ are formed in a second conductive layer, said first and said second ~~main~~ electrodes being separated from each other by material of the organic ambipolar semiconductor layer, and said first and said second ~~main~~ electrodes being separated from said control electrode by said organic ferroelectric layer.

5. (Previously presented) The non-volatile memory device according to claim 2, wherein the first conductive layer is a conductive polymer layer.

6. (Previously presented) The non-volatile memory device according to claim 5, wherein the conductive polymer layer is a PEDOT/PSS layer or a PANI layer.

7. (Previously presented) The non-volatile memory device according to claim 4, wherein the second conductive layer is a conductive polymer layer.

8. (Previously presented) The non-volatile memory device according to claim 7, wherein the conductive polymer layer is a PEDOT/PSS layer or a PANI layer.

9. (Previously presented) The non-volatile memory device according to claim 1, wherein the organic ferroelectric layer is a ferroelectric polymer or oligomer layer.

10. (Previously presented) The non-volatile memory device according to claim 9, wherein the ferroelectric polymer or oligomer layer is a layer comprising material selected from: $(CH2\text{-}CF2)_n$, $(CHF\text{-}CF2)_n$ $(CF2\text{-}CF2)_n$ or combinations thereof to form (random) copolymers including $(CH2\text{-}CF2)_n\text{-}(CHF\text{-}CF2)_m$ or $(CH2\text{-}CF2)_n\text{-}(CF2\text{-}CF2)_m$.

11. (Previously presented) The non-volatile memory device according to claim 1, wherein the organic ambipolar semiconductor

layer comprises a mixture of an n-type and a p-type semiconductor material.

12. (Previously presented) The non-volatile memory device according to claim 11, wherein the organic ambipolar semiconductor layer comprises a mixture of [6,6]-phenyl C61 butyric acid methyl ester and poly[2-methoxy,5-(3,7) dimethyl-octyloxy]-p-phenylene vinylene.

13. (Previously presented) The non-volatile memory device according to claim 1, wherein the organic ambipolar semiconductor layer comprises a single organic material.

14. (Previously presented) The non-volatile memory device according to claim 13, wherein the single organic material is poly(3,9-di-tert-butylindeno[1,2-b] fluorene).

15. (Previously presented) The non-volatile memory device according to claim 1, the memory device comprising a memory window, whereby said memory window depends on a ratio of electron current

and hole current.

16. (Previously presented) The non-volatile memory device according to claim 15, whereby said ratio of electron current and hole current is close to 0 or close to 1.

17. (Currently amended) A method for processing a non-volatile memory device, the method comprising acts of:

forming an organic ferroelectric layer in contact with at least two sides of a first electrode and a second electrode; and

forming an organic ambipolar semiconductor layer in contact with one side of each of the first electrode and the second electrode and at least two sides of a control electrode, said organic ambipolar semiconductor layer and said organic ferroelectric layer being at least partially in contact with each other.

18. (Currently amended) A non-volatile memory device comprising:

first and second electrodes;

a control electrode;

an organic ambipolar semiconductor layer in contact with three sides of said first and second electrodes; and

an organic ferroelectric layer in contact with one side of each said first and second electrodes, at ~~lest~~ least two sides of said control electrode and at least partially in contact with said organic ambipolar semiconductor layer.

19. (Previously presented) The device of claim 18, further comprising a planarization layer in contact with one side of said control electrode.